

## Curriculum Vitae Michael D. Jones

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### Education

Ph.D., Computer Science, University of Utah: December 2001. Dissertation: *Formal Verification of Parameterized Protocols on Branching Networks*. Advisor: Ganesh Gopalakrishnan.

M.S., Computer Science, Brigham Young University, August 1997. Thesis: *Representing Abstract Theories Using Predicate Types*, Advisor: Phillip J. Windley.

B.S., Computer Science, Mathematics Minor, Brigham Young University, April 1995.

### Appointments

July 2001. Assistant Professor, Dept. of Computer Science, Brigham Young U.

### Refereed Journal Publications

K. Seppi, M. Jones and P. Lamborn, "Guided model checking with a Bayesian Meta-Heuristic", *Fundamentae Informatica*. To appear in Fall 2005.

M. Jones and J. Sorber, "Parallel Search for LTL Violations", *Software Tools for Technology Transfer*, Vol 7(1), pp. 31-42. January 2005.

A. Mokkedem, R. Hosabettu, M. Jones and G. Gopalakrishnan, "Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem", *Formal Methods in System Design*, Vol 16(1), January 2000.

### Refereed Conference Publications

T. Bao and M. Jones. "Time-efficient Model Checking with Magnetic Disk", *Tools and Algorithms for the Construction and Analysis of Systems (TACAS 2005)*. Edinburgh, Scotland, April 2005.

M. Jones, D. Delorey and A. Benson. "Using Refinement to Show Compatibility" *Theorem Provers in Higher-Order Logic (TPHOLs 2004)*. Park City, Utah, September 2004.

B. Smith, K. Seamons and M. Jones “Responding to Policies at Run Time: The Design and Implementation of a Complete Strategy for Automated Trust Negotiation in TrustBuilder” *5th IEEE International Workshop on Policies for Distributed Systems and Networks*. Yorktown Heights, New York, June, 2004.

M. Jones and E. Mercer. “Explicit state model checking with Hopper” *11th International SPIN Workshop on Model Checking of Software*, Barcelona, Spain, April 2004.

M. Jones, E. Mercer, T. Boa, R. Kumar, P. Lamborn, “Benchmarking Explicit State Parallel Model Checkers”, *PDMC03: International Workshop on Parallel and Distributed Model Checking*. Boulder, Colorado, July 2003.

A. Weinzoepflen, M. Jones, D. Mery, D. Cansell and G. Gopalakrishnan, “Incremental proof of the producer/consumer property for the PCI protocol” *ZB2002: Formal Specification and Development in Z and B*. Grenoble, France, January 2002. Springer LNCS v.2272.

M. Jones and G. Gopalakrishnan, “Toward Automated Abstraction for Protocols Over Branching Networks,” *IEEE International High Level Design Validation and Test Workshop (HLDVT'00)*, Palo Alto, California, November 2000.

M. Jones and G. Gopalakrishnan, “Verifying Transaction Ordering Properties in Unbounded Bus Networks through Combined Deductive/Algorithmic Methods,” *Formal Methods in Computer-Aided Design (FMCAD'00)*, Austin, Texas, November 2000.

A. Jones, M. Jones, M. Clement and Q. Snell “Pyramid Broadcasting with Fast-Forward and Rewind,” *8th International Conference on Telecommunication Systems, Modeling and Analysis*, Nashville, Tennessee, March 2000.

A. Bunker, M. Jones. T. Larson and P. Windley, “Alexandria: A Tool for Hierarchical Verification,” *Formal Methods in Computer-Aided Design (FMCAD98)*, Palo Alto, California, November 1998. *Lecture Notes in Computer Science*, Springer-Verlag, Vol. 1522, pp. 515-522.

A. Bunker, M. Jones, T. Larson and P. Windley, “A Hierarchical Formal Verification Tool for Simple HDLs,” *Workshop on Libraries, Component Modeling and Quality Assurance*, Barcelona, Spain, 1997.

## **Other Publications**

M. Jones, “Adapting negative feedback in honey bee forager allocation to parallel LTL violation discovery”, *MASI 2003: Workshop on the Mathematics and Algorithms of Social Insects*. Atlanta, Georgia, December 2003. Poster session abstract.

M. Jones, P. Windley “Predicate Types for HOL,” *Theorem Provers in Higher-Order Logics (TPHOLs '97)*, Murray Hill, New Jersey, August 1997. Supplementary Proceedings.

P. Black, K. Hall, M. Jones, T. Larson and P. Windley, “A Brief Introduction to Formal Methods,” *IEEE Custom Integrated Circuits Conference*, 1996. Invited paper.

### **Funding**

“Design Technology for Protocols”, Funded by Strategic CAD Labs, Intel Corporation in the amount of \$24,000. April 2002.